Introduction

This technical note is intended to provide information about Kionix's 4 x 4 mm LGA packages and guidelines for developing PCB land pattern layouts. These guidelines are general in nature and based on recommended industry practices. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing techniques and the needs of varying end-use applications. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

Package Marking

- Marking font type : Arial
- Font size : 1.5 Point (0.56 mm height)
- Line space : 0.3 mm
- Text information
  - 1st line – Device name
  - 2nd line – Assembly Build Lot code
  - 3rd line – Date code (WWYY)
  - 4th line – Pin #1 Dot (0.5 mm diameter)

Note - All text lines shall be right justified.

Figure 1: 4x4 LGA package marking information.

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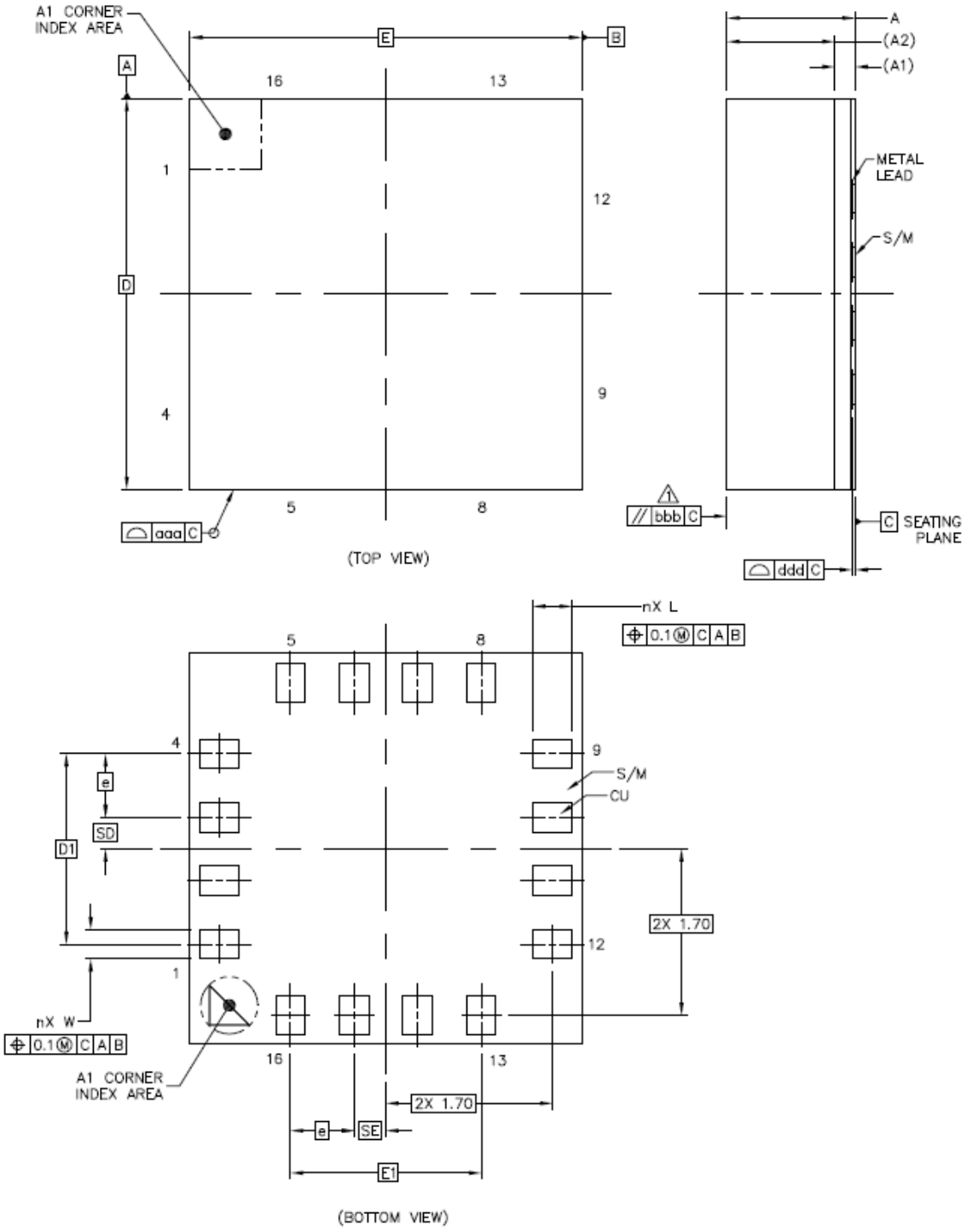
Package Outline and Dimensions

The following diagrams show the outline of the Kionix's LGA packages with dimensions and tolerances. All dimensions and tolerances conform to ASME Y14.5M-1994. All dimensions are in millimeters and angles are in degrees.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	1.31	1.35
SUBSTRATE THICKNESS	A1		0.21	REF
MOLD THICKNESS	A2		1.1	REF
BODY SIZE	D		4	BSC
	E		4	BSC
LEAD WIDTH	W	0.25	0.3	0.35
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.65	BSC
LEAD COUNT	n		16	
EDGE BALL CENTER TO CENTER	D1		1.95	BSC
	E1		1.95	BSC
BODY CENTER TO CONTACT BALL	SD		0.325	BSC
	SE		0.325	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

Figure 2: 16-pin 4 x 4 mm LGA package outline diagram with dimensions.

Typical LGA packages expose metal traces on the package sides; so no solder material should be allowed to contact the package sides.

PCB Layout Recommendations

Given the above package dimensions, the following guidelines are recommended:

The PCB should be designed with NSMD (Non-Solder Mask Defined) openings for the LGA land pattern. The LGA land pattern should be an identical mirror image of the bottom pattern of the LGA package.

The pin 1 indicator triangle that is exposed on the LGA substrate does not need to be soldered to the PCB and should be left floating.

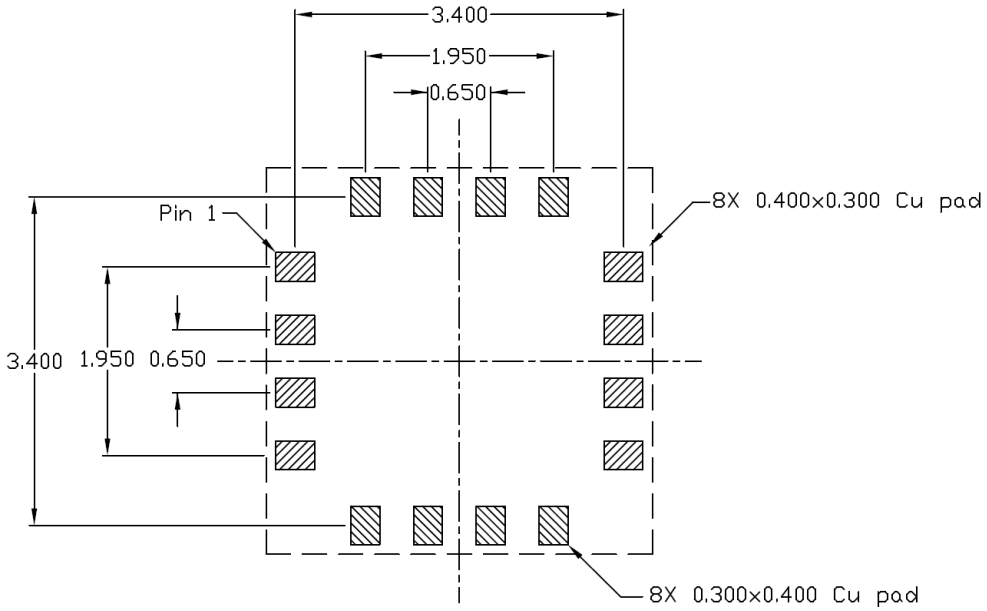


Figure 3: Example of a PCB land pattern for the 4 x 4 mm LGA package (Top view)

Using a 0.0635 mm solder mask around each pad (pad dimension + 0.1270 mm), the minimum solder mask web is 0.223 mm between I/O pads.

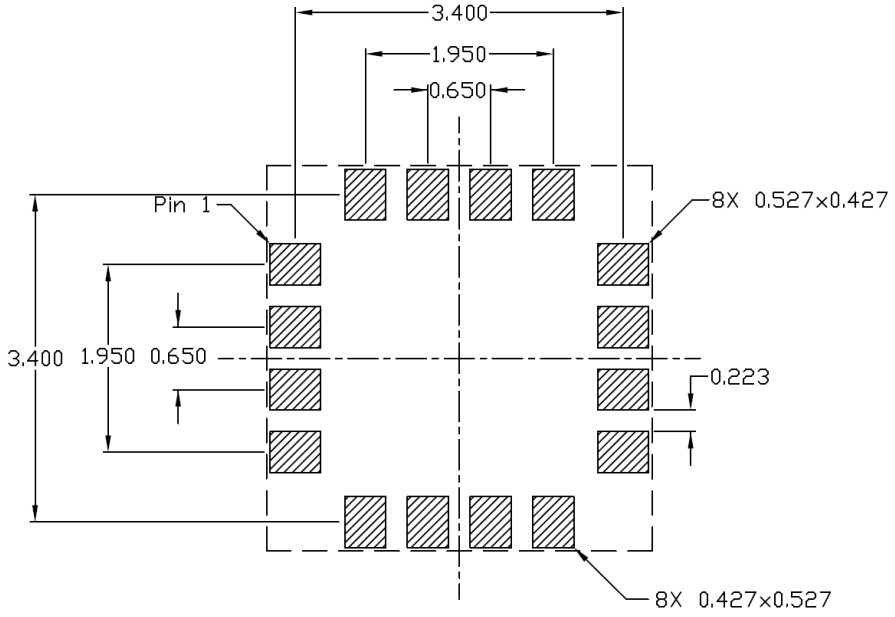


Figure 4: Example of solder mask for the 4 x 4 mm LGA package (Top view)

Solder Stencil Guidelines

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended. The recommended solder stencil thickness is 0.127 mm. The solder mask openings should be an identical mirror image of the bottom pattern of the LGA package with a 0.025mm corner radius to improve paste release.

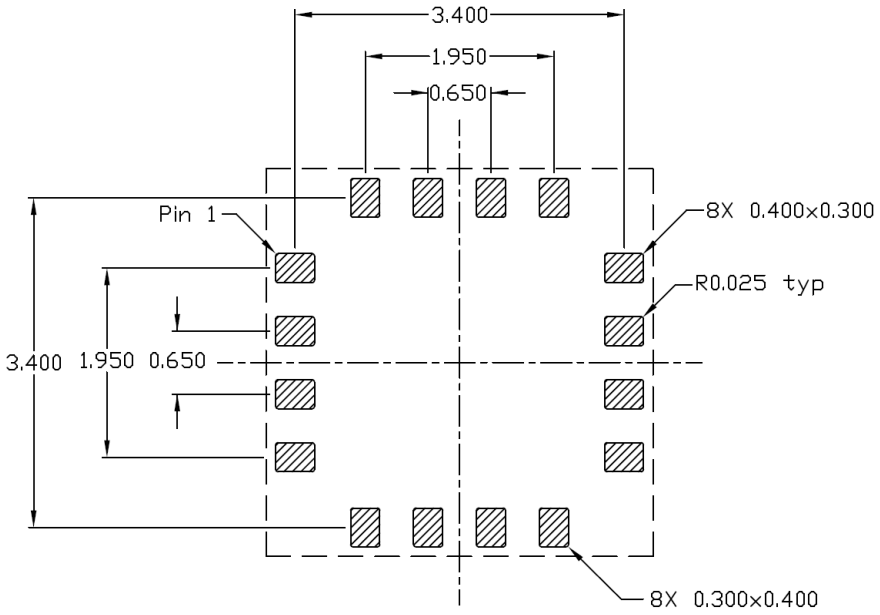


Figure 5: Example of a 16-pin 4 x 4 mm LGA solder stencil layout (Top view)

PCB Via and Trace Placement

Vias are not needed for thermal dissipation, as our part doesn't generate much heat. Therefore, only electrical vias are needed. If vias are not in the land pads, then capped, plugged, tented, un-capped or un-plugged vias can be used.

To ensure optimal performance, vias and traces should not be placed on the top layer directly beneath the sensor. The sensor should be mounted over a ground plane to minimize EMI from other signals. In the case PCB assemblies are stacked, there should be a ground plane over the sensor for the same reason.

The following figures illustrate an example of proper PCB via and trace placement. Obviously, each product will present its own physical limitations for sensor placement and trace routing. Therefore, these guidelines are general in nature. Engineering judgment should be used to try to avoid metal placement directly beneath the sensor on the same layer.

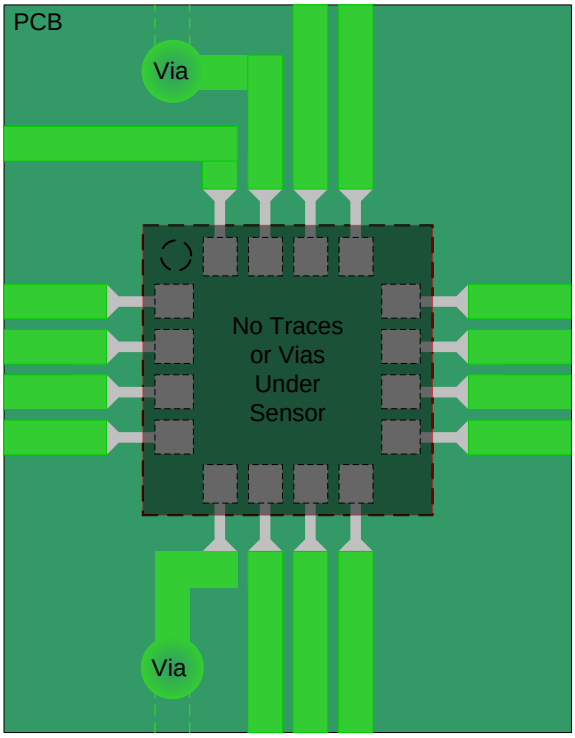


Figure 6: Via and Trace "Keep-out" (Top View)

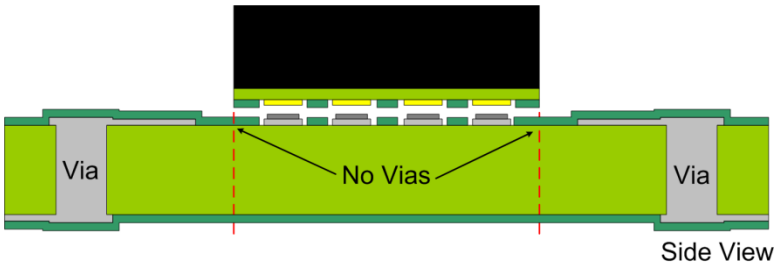


Figure 7: Via and Trace “Keep-out”
(Side View)

Tape and Reel Dimensions

The following section provides information on the tape and reel used for shipping Kionix's 4 x 4 mm LGA sensors.

Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter
LGA (4x4)	12mm	8mm	4mm	330mm

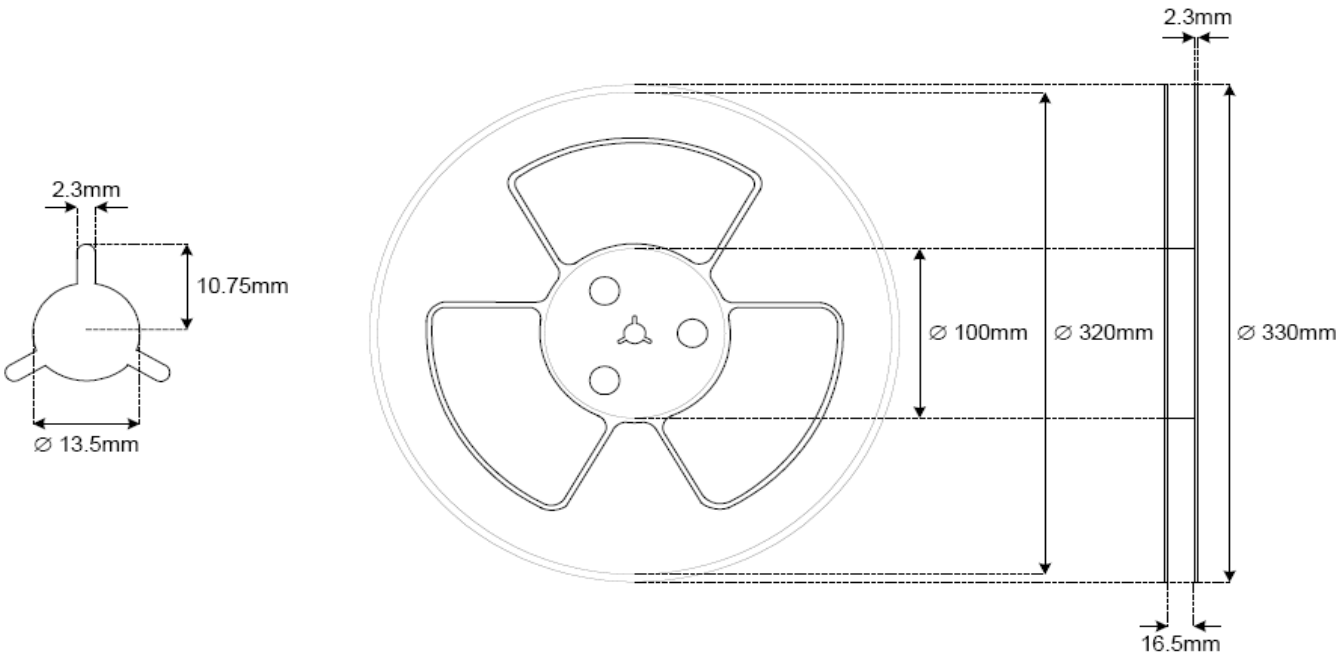
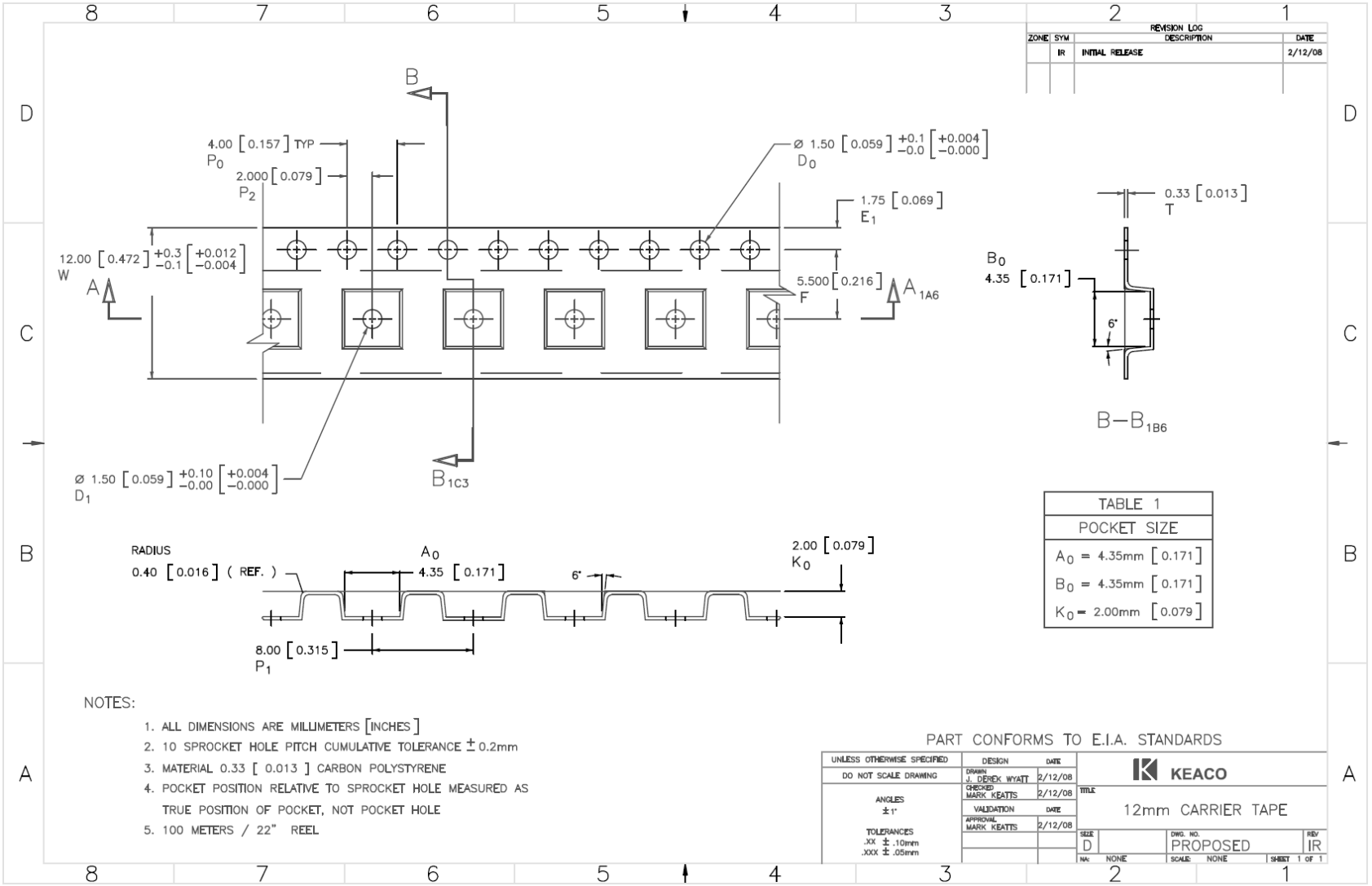


Figure 8: Dimensions of the reel



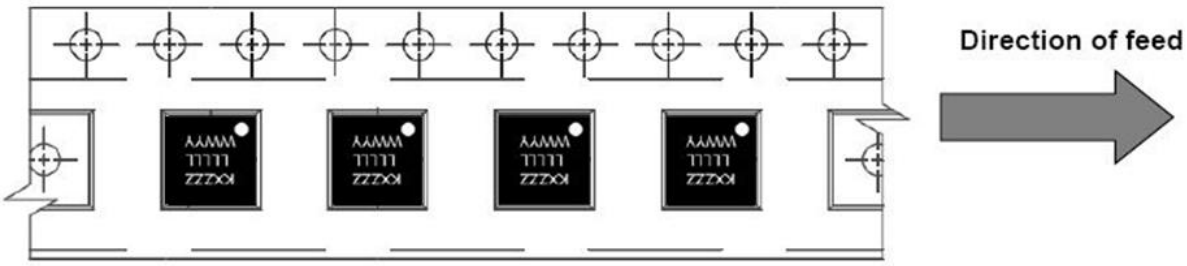


Figure 9: Orientation of the parts in the carrier tape and direction of feed

Revision History

Rev	Date	Description of Change
-	03-Jul-08	Initial release
1	09-Jun-10	Updated package dimension drawing
2	10-Aug-10	Added Traces, Vias section diagrams
3	15-Feb-12	Changed the orientation of the part in tape (Figure 7)
4	15-Oct-14	Added No solder on side of package recommendation.
5	10-July-15	Renamed document
6	19-Mar-19	Replaced accelerometer with sensor. Updated PCB Layout, Solder Stencil, and Via and Trace to current practices.