1. Introduction

This technical note is intended to provide information about the proper power-on procedure of the Kionix **KMX62, KMX63** sensors.

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{LOW}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{LOW}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the VDD ramp up time **T_{VDD}** be monotonic. To assure proper POR in all environmental conditions the application should be evaluated over the customer specified range of **VDD**, **VDD_{LOW}**, **T_{VDD}**, **T_{VDD_OFF}** and temperature as POR performance can vary depending on these parameters

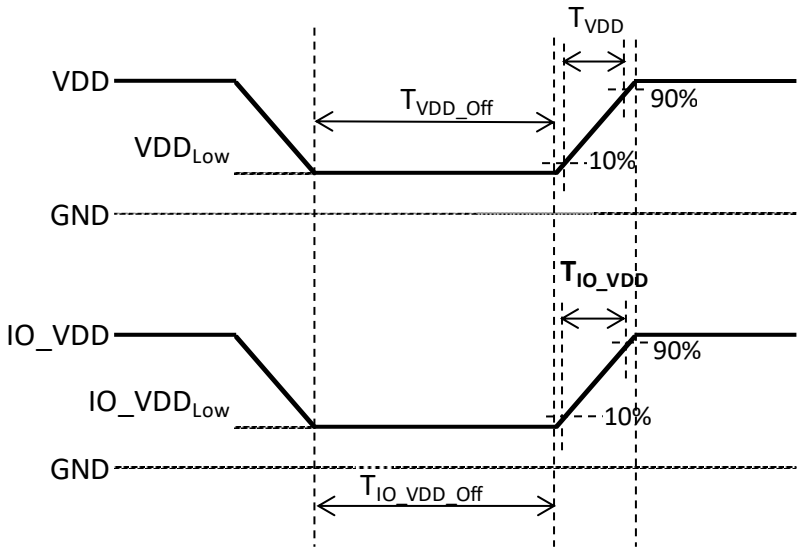

Figure 1: Power-On Reset Timing Diagram

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2. POR Performance

Bench Testing has demonstrated POR performance regions for a proper POR trigger. To assure POR trigger properly executes, setting operational thresholds consistent with **Error! Reference source not found.** below is recommended.

Parameters	Units	Min	Typical	Max
VDD rise time: T_{VDD}[1,2]	ms			5
IO_VDD rise time: T_{IO_VDD}[1,2]	ms			5
VDD off time: T_{VDD_OFF}[3,4]	ms	20		
IO_VDD off time: $T_{IO\_VDD\_OFF}$[3]	ms	20		
VDD low voltage: VDD_{LOW}[3,4]	mV			200
IO_VDD low voltage: IO_VDD_{LOW}[3]	mV			200
Software Reset Time[5]	ms		0.3	2
Power Up Time[6]	ms		20	50

Table 1: POR Performance

Notes:

1. VDD and IO_VDD must always be monotonic ramps without ambiguous state
2. T_{VDD} and T_{IO_VDD} rise from 10% to 90% of final value needs to be ≤ 5ms.
3. T_{VDD_OFF} and $T_{IO\_VDD\_OFF}$ are off time for VDD and IO_VDD rails respectively. To prevent the accelerometer from entering an ambiguous state, both VDD and IO_VDD need to be pulled down to GND (≤ 200mV) for duration of time ≥ 20ms.
4. It is important the user determines the timing (**T_{VDD_OFF}**) and threshold (**VDD_{LOW}**) levels by evaluating the performance in the specific system for which the device will be incorporated.
5. Software Reset Time is defined as time it takes to perform a RAM reboot routine following the setting of SRST bit to 1 in the CNTL1 register. The SRST bit will remain 1 until the RAM reboot routine is completed
6. Power Up Time is defined as time from VDD and IO_VDD become valid to device boot completion.

3. Software Reset

Issuing the Software Reset command after the device was powered up is recommended. This is effective against dynamic or non-liner behavior of a power supply or unexpected noise above normal on the power rail during a power up.

3.1. I2C Interface

3.1.1. I2C Slave Addresses for Software Reset

The Software Reset command should be sent to **two** special I2C slave addresses. The I2C slave address is set by 2 bits - the ADDR pin and an internal bit. An unsuccessful power-on may cause the internal value of the configuration address bit to be altered. The Table 2 below shows Slave Address #1 and #2 for devices with ADDR pin connected to IO_VDD. Note - the "Slave Address #1" in the table is the same as the slave address for normal operation.

Description	ADDR Pin	7-bit Slave Address for Normal Operation	7-bit Slave Address #1 for sending Software Reset command	7-bit Slave Address #2 for sending Software Reset command
I2C Wr	IO_VDD	0x0F	0x0F	0x0D

Table 2: I2C Slave Address #1 and #2 for Software Reset with ADDR pin at IO_VDD

The Table 3 below shows Slave Address #1 and #2 for devices with ADDR pin connected to VSS.

Description	ADDR Pin	7-bit Slave Address for Normal Operation	7-bit Slave Address #1 for sending Software Reset command	7-bit Slave Address #2 for sending Software Reset command
I2C Wr	VSS	0x0E	0x0E	0x0C

Table 3: I2C Slave Address #1 and #2 for Software Reset with ADDR pin at VSS

3.1.2. Software Reset Sequence following Power Up

a. Following the power up, write 0x00 to internal register 0x7F using Slave Address #1 as specified in Table 2 or Table 3 depending of the connection of ADDR pin. If command was acknowledged (ACK received), proceed to the next step while addressing the device using Slave Address #1. If ACK was not received, resend the command using Slave Address #2. If command was acknowledged, proceed to the next step while addressing the device using Slave Address #2. If command was not acknowledged again, the device should be power cycled.

Register Name	**Address**		**Value**	
	Hex	Binary	Hex	Binary
0x7F	**0x7F**	**0111 1111**	**0x00**	**0000 0000**

b. Write 0x00 to Control Register 2 (CNTL2). If NACK received, the device should be power cycled.

Register Name	**Address**		**Value**	
	Hex	Binary	Hex	Binary
CNTL2	**0x3A**	**0011 1010**	**0x00**	**0000 0000**

c. Write 0x80 to Control Register 1 (CNTL1) to initiate software reset, which performs the RAM reboot routine. If software reset command was acknowledged (ACK received), wait 2 milliseconds for completion of the Software Reset and proceed to the next step. If NACK received, the device should be power cycled.

Register Name	**Address**		**Value**	
	Hex	Binary	Hex	Binary
CNTL1	**0x39**	**0011 1001**	**0x80**	**1000 0000**

d. Read content of "Who am I" register (WHO_AM_I) using the normal I2C address (same as Slave Address #1). If value read is what is **0x18** (for KMX62) or **0x2D** (for KMX63), proceed to the next step. If not, the software reset has failed and the device should be power cycled.

Register Name	**Sensor**	**Address**		**Value**	
		Hex	Binary	Hex	Binary
WHO_AM_I	**KMX62**	**0x00**	**0000 0000**	**0x18**	**0001 1000**
	KMX63			**0x2D**	**0010 1101**

e. Read the content of Command Test Response (COTR) register. If read value is 0x55, the device operation can be started. If read value is not 0x55, the software reset has failed and the device should be power cycled.

Register Name	**Address**		**Value**	
	Hex	Binary	Hex	Binary
COTR	**0x3C**	**0011 1100**	**0x55**	**0101 0101**

3.1.3. Software Reset Timing Diagram

Figure 2 below shows an example of executing Software Reset sequence outlined section 0 following a power up. The first attempt is to communicate with device using Slave Address #1 as specified in Table 2 or Table 3 depending of the connection of ADDR pin. If attempt is unsuccessful, the second attempt is to communicate with device using Slave Address #2. Two milliseconds wait time is required for completion of Software Reset before proceeding.

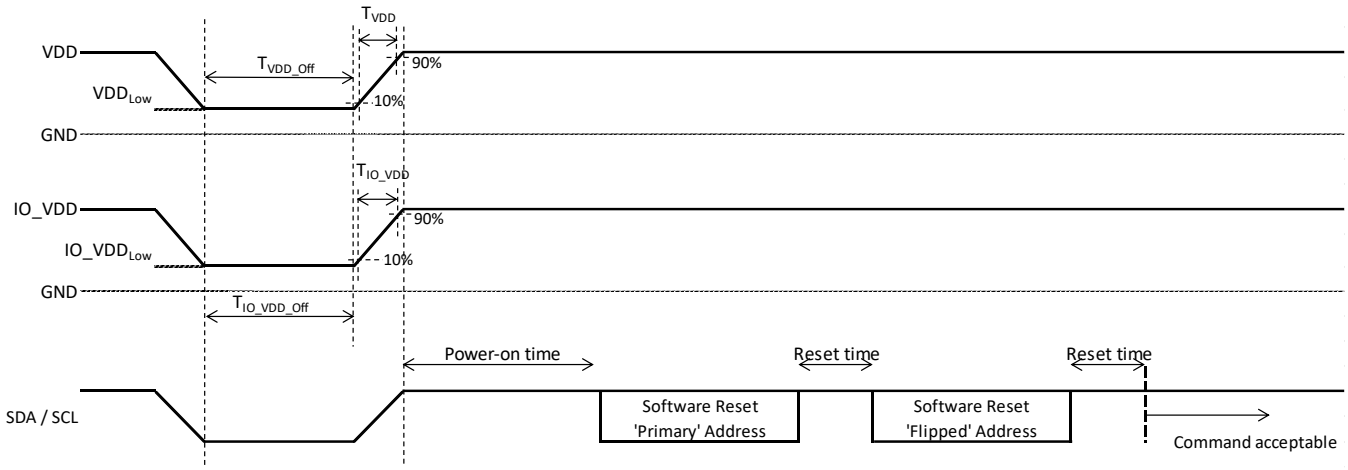

Figure 2. Power-On Timing Diagram followed by sending of two I2C Software Reset Commands

The data provided by Kionix is intended for initial customer design guidance only. Kionix POR testing looks at a finite number of test configurations. Each customer application will have varying input sensor parameters (electrical, mechanical, and environmental) that will be different than the configurations tested by Kionix. Each customer utilizing the sensor will need to properly validate the sensor (including POR function) within their application under their specific use cases to ensure it responds as required.