Replacing KX022 and KX122 with KX126 Accelerometer

Introduction

The purpose of this application note is to illustrate how the Kionix KX126 accelerometer can replace an existing Kionix KX022 or KX122 accelerometer.

Side-by-Side Comparison

The following are key side-by-side comparisons between the KX022, KX122, and KX126 accelerometers. Typical values are shown, unless otherwise indicated.

Package Information

		KX022	KX122	KX126
Parameter	**Units**			
Sensing Axes (Accel)		XYZ 3-axis	XYZ 3-axis	XYZ 3-axis
Package Size	mm	2x2x0.9	2x2x0.9	2x2x0.9
Package Type		LGA	LGA	LGA
Pins		16	16	16

Features

		KX022	KX122	KX126
Parameter	**Units**			
Low Power Mode		Yes	Yes	Yes
Self-test		Yes	Yes	Yes
Wake-up		Yes	Yes	Yes*
Back-to-sleep		No	No	Yes
Freefall Detection		No	Yes	Yes
Tap, Double-Tap Detection		Yes	Yes	Yes
Tilt Orientation Detection		Yes	Yes	Yes
Pedometer		No	No	Yes
Sample Buffer (FIFO)	Bytes	256	2048	2048*

* See Key Differences section for further details

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Electrical Specifications

			KX022	KX122	KX126
Parameter		**Units**			
Supply Voltage (VDD)		V	1.71–3.6	1.71–3.6	1.71–3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.7–3.6	1.7–3.6	1.7–3.6
Current Consumption (Typical)	High Resolution Mode (RES = 1)	µA	145	145	145
	Low Power Mode (RES = 0)	µA	10	10	10
	Standby	µA	0.9	0.9	0.9
I^2C Communication Rate (max)		MHz	3.4	3.4	3.4
SPI Communication Rate (max)		MHz	10	10	10
Output Data Rate [ODR] (max)		KHz	1.6	25.6	25.6

Environmental

		KX022	KX122	KX126
Parameter	**Units**			
Supply Voltage (VDD)	V	-0.5–3.63	-0.5–3.63	-0.3–3.63
Operating Temperature Range	°C	-40–85	-40–85	-40–85
Storage Temperature Range	°C	-55–150	-55–150	-55–150
Mechanical Shock (powered and unpowered)	g	5000 for 0.5ms 10000 for 0.2ms	5000 for 0.5ms 10000 for 0.2ms	5000 for 0.5ms 10000 for 0.2ms
ESD (HBM)	V	2000	2000	2000

Accelerometer Mechanical

			KX022	KX122	KX126
Parameter		**Units**			
Operating Temperature Range		°C	-40–85	-40–85	-40–85
Zero-g Offset		mg	±25	±25	±25
Zero-g Offset Variation from RT over Temp.		mg/°C	±0.2	±0.2	±0.2
Sensitivity (Typical)	GSEL1=0, GSEL0=0 (±2g)	counts/g	16384	16384	16384
	GSEL1=0, GSEL0=1 (±4g)	counts/g	8192	8192	8192
	GSEL1=1, GSEL0=0 (±8g)	counts/g	4096	4096	4096
Sensitivity Variation from RT over Temp.		%/°C	0.01	0.01	0.01
Self-Test Output change on Activation		g	0.5	0.5	0.5
Mechanical Resonance (-3dB)		Hz	-	4000 (xy) 2800 (z)	4000 (xy) 2800 (z)
Non-Linearity		% of FS	0.6	0.6	0.6
Cross Axis Sensitivity		%	2	2	2
Noise (RMS at 50Hz)		mg	0.7	0.7	0.7

Sensor Output Registers (Primary)

Addr	KX022	KX122	KX126
00	XHP_L	XHP_L	MAN_ID
01	XHP_H	XHP_H	PART_ID
02	YHP_L	YHP_L	XHP_L
03	YHP_H	YHP_H	XHP_H
04	ZHP_L	ZHP_L	YHP_L
05	ZHP_H	ZHP_H	YHP_H
06	XOUT_L	XOUT_L	ZHP_L
07	XOUT_H	XOUT_H	ZHP_H
08	YOUT_L	YOUT_L	XOUT_L
09	YOUT_H	YOUT_H	XOUT_H
0A	ZOUT_L	ZOUT_L	YOUT_L
0B	ZOUT_H	ZOUT_H	YOUT_H
0C	COTR	COTR	ZOUT_L
0D	---	---	ZOUT_H
0E	---	---	PED_STPL
0F	WHO_AM_I	WHO_AM_I	PED_STPH
10	TSCP	TSCP	COTR
11	TSPP	TSPP	WHO_AM_I
12	INS1	INS1	TSCP
13	INS2	INS2	TSPP
14	INS3	INS3	INS1
15	STAT	STAT	INS2
16	Kionix Reserved	Kionix Reserved	INS3
17	INT_REL	INT_REL	STAT
18	CNTL1*	CNTL1*	Kionix Reserved
19	CNTL2*	CNTL2*	INT_REL
1A	CNTL3*	CNTL3*	CNTL1[3]
1B	ODCNTL*	ODCNTL*	CNTL2[3]
1C	INC1*	INC1*	CNTL3[3]
1D	INC2*	INC2*	CNTL4[3]
1E	INC3*	INC3*	CNTL5[3]
1F	INC4*	INC4*	ODCNTL[3]
20	INC5*	INC5*	INC1[3]
21	INC6*	INC6*	INC2[3]
22	TILT_TIMER*	TILT_TIMER*	INC3[3]
23	WUFC*	WUFC*	INC4[3]
24	TDTRC*	TDTRC*	INC5[3]
25	TDTC*	TDTC*	INC6[3]
26	TTH*	TTH*	INC7[3]
27	TTL*	TTL*	TILT_TIMER[3]
28	FTD*	FTD*	TDTRC[3]
29	STD*	STD*	TDTC[3]
2A	TLT*	TLT*	TTH[3]

Addr	KX022	KX122	KX126
2B	TWS*	TWS*	TTL[3]
2C	Kionix Reserved	FFTH*	FTD[3]
2D	Kionix Reserved	FFC*	STD[3]
2E	Kionix Reserved	FFCNTL*	TLT[3]
2F	Kionix Reserved	Kionix Reserved	TWS[3]
30	ATH*	ATH*	FFTH[3]
31	Kionix Reserved	Kionix Reserved	FFC[3]
32	TILT_ANGLE_LL*	TILT_ANGLE_LL*	FFCNTL[3]
33	TILT_ANGLE_HL*	TILT_ANGLE_HL*	Kionix Reserved
34	HYST_SET*	HYST_SET*	TILT_ANGLE_LL[3]
35	LP_CNTL*	LP_CNTL*	TILT_ANGLE_HL[3]
36	Kionix Reserved	Kionix Reserved	HYST_SET[3]
37	Kionix Reserved	Kionix Reserved	LP_CNTL[3]
38	Kionix Reserved	Kionix Reserved	Kionix Reserved
39	Kionix Reserved	Kionix Reserved	Kionix Reserved
3A	BUF_CNTL1*	BUF_CNTL1*	Kionix Reserved
3B	BUF_CNTL2*	BUF_CNTL2*	Kionix Reserved
3C	BUF_STATUS_1	BUF_STATUS_1	WUFTH[3]
3D	BUF_STATUS_2	BUF_STATUS_2	BTSWUFTH[3]
3E	BUF_CLEAR	BUF_CLEAR	BTSTH[3]
3F	BUF_READ	BUF_READ	BTSC[3]
40	Kionix Reserved	Kionix Reserved	WUFC[3]
41	Kionix Reserved	Kionix Reserved	PED_WM_L[3]
42	Kionix Reserved	Kionix Reserved	PED_WM_H[3]
43	Kionix Reserved	Kionix Reserved	PED_CNTL1[3]
44	Kionix Reserved	Kionix Reserved	PED_CNTL2[3]
45	Kionix Reserved	Kionix Reserved	PED_CNTL3[3]
46	Kionix Reserved	Kionix Reserved	PED_CNTL4[3]
47	Kionix Reserved	Kionix Reserved	PED_CNTL5[3]
48	Kionix Reserved	Kionix Reserved	PED_CNTL6[3]
49	Kionix Reserved	Kionix Reserved	PED_CNTL7[3]
4A	Kionix Reserved	Kionix Reserved	PED_CNTL8[3]
4B	Kionix Reserved	Kionix Reserved	PED_CNTL9[3]
4C	Kionix Reserved	Kionix Reserved	PED_CNTL10[3]
4D	Kionix Reserved	Kionix Reserved	SELF_TEST
4E-4F	Kionix Reserved	Kionix Reserved	Kionix Reserved
5A	Kionix Reserved	Kionix Reserved	BUF_CNTL1*
5B	Kionix Reserved	Kionix Reserved	BUF_CNTL2*
5C	Kionix Reserved	Kionix Reserved	BUF_STATUS_1
5D	Kionix Reserved	Kionix Reserved	BUF_STATUS_2
5E	Kionix Reserved	Kionix Reserved	BUF_CLEAR
5F	Kionix Reserved	Kionix Reserved	BUF_READ
60	SELF_TEST	SELF_TEST	Kionix Reserved
61-69	Kionix Reserved	Kionix Reserved	Kionix Reserved
6A	Kionix Reserved	Kionix Reserved	Kionix Reserved

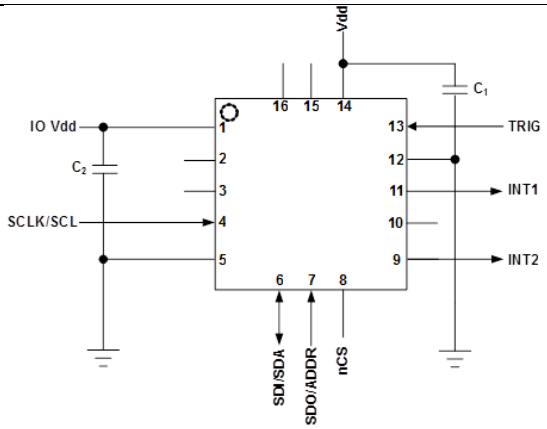
Table 1: Register comparison, KX022 v KX122 v KX126

Note:
For a detail about the function of each of the registers in Table 1, please refer to the product specs listed on their individual product pages from our affiliates or on the Kionix website: KX022, KX122, KX126

Pin Compatibility

The KX022/122 accelerometer can be easily replaced by a KX126 accelerometer for either an I2C or SPI interface application. From a hardware perspective, the KX022, KX122, and KX126 have identical pad/pin layouts and package sizes, measuring 2x2x0.9mm.

KX022/122/126



Pin	Name	Description
1	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
3	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
4	SCLK/SCL	SPI and I^2C Serial Clock
5	GND	Ground
6	SDI/SDA	SPI Data input / I2C Serial Data
7	SDO/ADDR	Serial Data Out pin during 4 wire SPI communication and part of the device address during I2C communication.
8	nCS	SPI enable / I2C mode select. Connect to GND for SPI enabled, I2C communication disabled. Connect to IO_VDD for SPI disabled, I2C communication enabled. Do not leave floating.
9	INT2	Physical Interrupt 2. Leave floating if not used.
10	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
11	INT1	Physical Interrupt 1. Leave floating if not used.0
12	GND	Ground
13	TRIG	Trigger pin for FIFO buffer control – Connect to GND when not using external trigger option.
14	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
16	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating

Figure 1: Pin Description for KX022, KX122, and KX126

Key Similarities

- KX022, KX122, and KX126 accelerometer outputs are all 16-bit.
- KX022 and KX122 share identical register mappings, with the exception that the KX122 adds registers / bits that were previously reserved in the KX022 to support additional features, such as free fall and a larger buffer. Any software register control currently written for the KX022, will work seamlessly with the KX122. Interrupt control and configurations registers are identical (mapping).
- KX126 has added MAN_ID and PART_ID registers, pedometer and back-to-sleep engines related config registers/bits.
- Since KX022 / KX122 and KX126 share many of the same embedded engines, any software currently controlling the KX022 / KX122 application engines, will work for the KX126 with only slight modification. Changes required will primarily apply to register addresses and threshold settings.

Key Differences

New Features

- The KX022 is a first-generation high performance, feature-rich accelerometer. The KX122 and KX126 are the second and the third generation (respectively) that additionally offer:
  - **Free fall Engine** (KX122, KX126): An embedded application engine that detects free fall events.
  - **Sample Rates**
    - KX122 and KX126 extends the sampling rate to 25.6kHz in High Resolution mode and KX126 extends the sampling rate to 400Hz in Low Power Mode. See table below for details.

	Low Power Mode			High Resolution Mode		
ODR (Hz)	KX022	KX122	KX126	KX022	KX122	KX126
0.781						
1.563						
3.125						
6.25						
12.5						
25						
50						
100						
200						
400						
800						
1600						
3200						
6400						
12800						
25600						

- **Back-to-Sleep Engine**
  - KX126 offers a back-to-sleep engine that can be configured independently of the wake-up-engine.
- **Wake-up / Back-to-Sleep Resolution**
  - The wake-up resolution for KX022 and KX122 is 62.5mg/count. The resolution for both, the Wake-up and Back-to-sleep engines on KX126 is 3.9mg/count.
- **Pedometer Engine**
  - KX126 offers an integrated pedometer (step counter) engine with overflow, watermark, and increment interrupts.

Buffer Operation *(continued on next page)*

- Buffer Size
  - KX022 buffer size is 256 bytes – up to 84 (8-bit) and 41 (16-bit) samples can be stored.
  - While KX122 and KX126 feature 2048-bytes buffer, the number of samples stored in the full buffer differs as following:
    - KX122: up to 681 (8-bit) and 340 (16-bit) samples can be stored
    - KX126: up to 683 (8-bit) and 342 (16-bit) samples can be stored
- Buffer Auto-Clear
  - KX022 doesn't clear the content of the buffer after buffer is disabled. The content of the buffer will remain the same until (1) the data is read out or (2) the buffer is cleared.
  - KX122 and KX126 clears the content of the buffer after buffer is disabled. The content of the buffer will remain the same until (1) the data is read out or (2) the buffer is cleared or (3) the buffer is disabled.
- Data Loss Consideration
  - For KX022 and KX122, no new data is stored to the buffer when buffer is being read. To prevent data loss, the buffer read should be synchronized to internal clock (e.g. using DRDY interrupt) and be completed within 1/ODR cycle.
  - KX126 prevents data loss by continuing to buffer data even while being read.

Sample Threshold

(SMP_TH) – controls the number of samples that will trigger a watermark interrupt or will be saved prior to a trigger event (see next page)

- Sample threshold bits (SMP_TH) have been expanded from 7 bits in KX022 to 9 bits to support the larger buffer of the KX122 and KX126
- In the KX122 and KX126, expanded bits SMP_TH[9:7] can be found in BUF_CNTL2[3:2]

KX022

BUF_CNTL1

Read/write control register that controls the buffer sample threshold. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
-	SMP_TH6	SMP_TH5	SMP_TH4	SMP_TH3	SMP_TH2	SMP_TH1	SMP_TH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x3Ah			

Figure 2: KX022 SMP_TH Register/Bit Mapping

KX122/KX126

BUF_CNTL1

The Buffer Control 1 (BUF_CNTL1) register controls the buffer sample threshold. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SMP_TH7	SMP_TH6	SMP_TH5	SMP_TH4	SMP_TH3	SMP_TH2	SMP_TH1	SMP_TH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x5A			

BUF_CNTL2

The Buffer Control 2 (BUF_CNTL2) register controls sample buffer operation. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BUFE	BRES	BFIE	0	SMP_TH9	SMP_TH8	BM1	BM0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x5B			

Figure 3: KX122/KX126 SMP_TH Register/Bit Mapping (Note: The Register Addresses 0x5A and 0x5B are valid for KX126 sensor. For KX122, the addresses are 0x3A and 0x3B respectively)

Sample Level

(SMP_LEV) – reports the number of data bytes that have been stored in the sample buffer

- In the KX122, sample level bits (SMP_LEV) have been expanded to 11 bits <0:10> to support the larger buffer
- In the KX126, sample level bits (SMP_LEV) have been expanded to 12 bits <0:11> for even further control
- Like the KX022, bits SMP_LEV[7:0] still exist in BUF_STATUS_1
- In the KX122, the expanded bits SMP_LEV[10:8] can be found in BUF_STATUS_2[2:0]
- In the KX126, the expanded bits SMP_LEV[11:8] are found in BUF_STATUS_2[2:0]

KX022

BUF_STATUS_1

This register reports the status of the sample buffer.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2	SMP_LEV1	SMP_LEV0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x3Ch		

Figure 4: KX022 SMP_LEV Register/Bit Mapping

KX122

BUF_STATUS_1

Buffer Status 1: This register reports the status of the sample buffer.

R	R	R	R	R	R	R	R
SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2	SMP_LEV1	SMP_LEV0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Address: 0x3C		

BUF_STATUS_2

Buffer Status 2: This register reports the status of the sample buffer trigger function.

R	R	R	R	R	R	R	R
BUF_TRIG	0	0	0	0	SMP_LEV10	SMP_LEV9	SMP_LEV8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Address: 0x3D		

Figure 5: KX122 SMP_LEV Register/Bit Mapping

KX126

BUF_STATUS_1 and BUF_STATUS_2

Buffer Status: These register reports the status of the sample buffer. Note that BUF_STATUS_1 and BUF_STATUS_2 registers may have a delay of up to 1 µsec to update the sample level after a buffer read.

R	R	R	R	R	R	R	R	BUF_STATUS_1
SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2	SMP_LEV1	SMP_LEV0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x5C			

R	R	R	R	R	R	R	R	BUF_STATUS_2
BUF_TRIG	0	0	0	SMP_LEV11	SMP_LEV10	SMP_LEV9	SMP_LEV8	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x5D			

Figure 6: KX126 SMP_LEV Register/Bit Mapping

WHO AM I

WHO_AM_I Register will report a different value to discern between Kionix sensors. See table below.

Part	Register	Address	Type	Value
KX022	WHO_AM_I	0x0F	Read Only	0x14
KX122	WHO_AM_I	0x0F	Read Only	0x1B
KX126	WHO_AM_I	0x11	Read Only	0x38

Power Up Time

The typical *Power Up Time*, which is from VDD valid to device boot completion, varies slightly from the KX022 to the KX122 / KX126. The typical times for the KX122 / KX126 are 20ms vs KX022 of 10ms, however, both have a maximum limit of 50ms.

The Kionix Advantage

Kionix technology provides for X, Y, and Z-axis sensing on a single, silicon chip. One accelerometer can be used to enable a variety of simultaneous features including, but not limited to:

Hard Disk Drive protection
Vibration analysis
Tilt screen navigation
Sports modeling
Theft, man-down, accident alarm
Image stability, screen orientation & scrolling
Computer pointer
Navigation, mapping
Game playing
Automatic sleep mode

Theory of Operation

Kionix MEMS linear tri-axis accelerometers function on the principle of differential capacitance. Acceleration causes displacement of a silicon structure resulting in a change in capacitance. A signal-conditioning CMOS technology ASIC detects and transforms changes in capacitance into an analog output voltage, which is proportional to acceleration. These outputs can then be sent to a micro-controller for integration into various applications.

For product summaries, specifications, and schematics, please refer to the Kionix MEMS accelerometer product sheets at http://www.kionix.com/parametric/Accelerometers